IN THE CLAIMS:

Please amend Claims 1, 8-13, 20-24, cancel Claims 25-32, and add new Claims 33-42 as follows.

1. (Amended) A microelectronic system comprising at least one package having:

at least one substrate having aligned global alignment marks formed on an alignment pattern irradiated on the at least one substrate; and

first and second circuit systems, each of said first and second circuit systems having means for wirelessly communicating with each other through said at least one substrate, wherein said first and second systems are aligned via said global alignment marks.

8. (Amended) The microelectronic system according to Claim 1, wherein the package is fabricated by an alignment process which includes the step of:

providing a photoresist on a top and bottom side of a substrate of said at least one substrate;

irradiating said photoresist from at least one side of said substrate to form the alignment pattern on said top and bottom side of said substrate;

etching said alignment pattern to form said global alignment marks on said top and bottom sides of said substrate; and

providing at least one communication device on one side of said substrate using at least one global alignment mark as a reference point.

9. (Amended) The microelectronic system according to Claim 1, wherein the first and second circuit systems include first and second interconnection structures for interconnecting components of the first and second circuit systems, respectively.

10. (Amended) The microelectronic system according to Claim 8, wherein the first and second interconnection structures are connected to the at least one substrate.

11. (Amended) The microelectronic system according to Claim 1, wherein the at least one substrate is aligned via said global alignment marks for aligning a substrate of the at least one substrate with global alignment marks of another substrate

12. (Amended) The microelectronic system according to Claim 1, wherein the circuitry package is fabricated by an alignment process which includes the steps of:

providing an opaque layer on one side of a substrate of said at least one substrate;

providing a photoresist on said opaque layer on one side of said substrate;

irradiating said photoresist from at least the one side of said substrate to form a first alignment pattern of said alignment pattern on said one side of said substrate;

etching said first alignment pattern to form a first set of global alignment marks of said global alignment marks on said one side of said substrate;

providing a photoresist on the other side of said at least one substrate;

irradiating said first alignment pattern from at least the one side of said substrate to form a second alignment pattern of said alignment patter on the other side of said substrate;

etching said second alignment pattern to form a second set of global alignment marks of said global alignment marks on the other side of said substrate, wherein the first and second sets of global alignment marks align with respect to each other; and

providing at least one communication device on said one side of said substrate using at least one global alignment mark from the first and second sets of global alignment marks as a reference point.

13. (Amended) A circuitry package comprising:

at least one substrate having aligned global alignment marks formed on an alignment pattern irradiated on the at least one substrate; and

first and second circuit systems, each of said systems having means for wirelessly communicating with each other through said at least one substrate, wherein said first and second systems are aligned via said global alignment marks for facilitating said wireless communication.

20. (Amended) The circuitry package according to Claim 13, wherein the package is fabricated by an alignment process which includes the step of:

providing a photoresist on a top and bottom side of a substrate of said at least one substrate;

irradiating said photoresist from at least one side of said substrate to form the alignment pattern on said top and bottom side of said substrate;

etching said alignment pattern to form said global alignment marks on said top and bottom sides of said substrate; and

providing at least one communication device on one side of said substrate using at least one global alignment mark as a reference point.

21. (Amended) The circuitry package according to Claim 13, wherein the first and second circuit systems include first and second interconnection structures for interconnecting components of the first and second circuit systems, respectively.

22. (Amended) The circuitry package according to Claim 21, wherein the first and second interconnection structures are connected to the at least one substrate.

23. (Amended) The circuitry package according to Claim 13, wherein the at least one substrate is aligned via said global alignment marks for aligning the a substrate of the at least one substrate with global alignment marks of another substrate.

24. (Amended) The circuitry package according to Claim 13, wherein the circuitry package is fabricated by an alignment process which includes the steps of:

providing an opaque layer on one side of a substrate of said at least one substrate;

providing a photoresist on said opaque layer on one side of said substrate;

irradiating said photoresist from at least the one side of said substrate to form a first alignment pattern on said one side of said substrate;

etching said first alignment pattern of said alignment pattern to form a first set of global alignment marks of said global alignment marks on said one side of said substrate;

providing a photoresist on the other side of said substrate;

irradiating said first alignment pattern from at lest the one side of said substrate to from a second alignment pattern on the other side of said substrate;

etching said second alignment pattern to from a second set of global alignment marks of said global alignment marks on the other side of said substrate, wherein the first and second sets of global alignment marks align with respect to each other; and

providing at least one communication device on said one side of said substrate using at least one global alignment mark from the first and second sets of global alignment marks as a reference point.

33. (New) The microelectronic system according to Claim 1, wherein a substrate of said at least one substrate has a first set of global alignment marks on a top surface of the substrate and a second set of global alignment marks discrete from and aligned with the first set of global alignment marks on the bottom surface of the substrate.

34. (New) The microelectronic system according to Claim 33, wherein the first set of global alignment marks and the second set of global alignment marks are formed substantially simultaneously.

35. (New) The microelectronic system according to Claim 1, wherein a first and second substrate of the at least one substrate are in surface to surface contact.

36. (New) The microelectronic system according to Claim 1, wherein the first and

second circuit systems are positioned on top and bottom surfaces, respectively, of a substrate of the at least one substrate.

37. (New) The microelectronic system according to Claim 36, wherein the first and second circuit systems are separated by a distance that is less than the distance between the top and bottom surface of the substrate.

38. (New) The circuitry package according to Claim 13, wherein a substrate of said at least one substrate has a first set of global alignment marks on a top surface of the substrate and a second set of global alignment marks discrete from and aligned with the first set of global alignment marks on the bottom surface of the substrate.

39. (New) The circuitry package according to Claim 13, wherein the first set of global alignment marks and the second set of global alignment marks are formed substantially simultaneously.

40. (New) The circuitry package according to Claim 39, wherein a first and second substrate of the at least one substrate are in surface to surface contact.

41. (New) The circuitry package according to Claim 13, wherein the first and second circuit systems are positioned on top and bottom surfaces, respectively, of a substrate of the at least one substrate.

42. (New) The circuitry package according to Claim 41, wherein the first and second circuit systems are separated by a distance that is less than the distance between the top and bottom surfaces of the substrate.